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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Christopher J Reckamp
Vedder Price Kaufman & Kammholz
222 North LaSalle Street
Chicago, IL 60601

EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/471,877	SFARTI ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-13 and 20-27* is/are allowed.

6)☒ Claim(s) *1-6,14,18,19 and 28-33* is/are rejected.

7)☒ Claim(s) *15-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 December 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-33 are presented for examination. Upon further review and new search, Sakugawa (6,684,278) is cited and used for showing the teaching of the processing the memory request at memory rate (see discussion below). Applicant is welcome to provide feedback in the next response.

2. Claims 1-4, 14,18,19, 28-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wandler et al. (5,991,833) in view of Sakugawa (6,684,278) .

3. As to claims 1,28, Wandler disclosed a system, comprising t at least :

a) integrating a central processing unit [CPU] with a north bridge [north bridge] on to a single substrate [10] (see col.6, lines 5-7) that the central processing unit [25] is directly coupled to the north bridge via internal bus [17] (see fig.2 [25][50][17]);

b)providing memory access requests from the central processing unit to the north gate at a rate of the CPU (e.g. see fig.2 [CPU Bus 17], see the memory accesses in col.6, lines 17-22);

c)buffering , in the north bridge [50], the memory access requests (e.g. see fig.4 [508][510] see the CPU-memory read/write queues for storing the requests in col.11, lines 55-67, col.12, lines 1-25);

d)processing by north bridge the access requests (see fig.4 [508][510] see the CPU-memory read/write queues for storing the requests in col.11, lines 55-67, col.12, lines 1-25).

4. Wandler did not specifically show his requests were processed at a rate of memory as claimed. However, Sakugawa disclosed a system for processing requests where a memory controller 2 is shifted to the waiting state in response to the memory access request from a cup [CPU] which was allowed to be operated at a low speed, the external device 32 which is to be operated at a high speed must wait for a period equivalent to the waiting time of the memory controller 2 (see the waiting period of the memory controller in col. 3, lines 1-14, col.5 lines 5-46, see also col.7, lines 5-25). It would have been obvious to one of ordinary skill in the art to use Sakugawa in Wandler for processing the request at a memory rate as claimed because the use of Sakugawa could provide Wandler the processing capability to accept different rate of a predetermined memory device, and it could be achieved by defining the memory control parameters of Sakugawa , such as memory width, and read/write cycles, into Wandler, such that the memory requests at a predetermined memory rate could be recognized by Wandler, and because one of ordinary skill in the art should be able to recognize the need of processing the requests at a memory rate as Wandler also taught a retrying cycle for read/write requests if the memory was busy (e.g. see col.3, lines 22-30) which was a suggestion of processing the request at the speed condition of the memory, and thereby allowing the bus to be freed for other access cycles, and for the above reasons, provided a motivation.

5. As to claim 2, Wandler also included at least :

a)integrating he south bridge on the substrate with CPU and north bridge (e.g. see PCI bus in fig.2, see also col.6, lines 5-7 for integrating the north bridge into CPU);

b)buffering the requests in the north bridge (e.g. see the request received by north bridge from south bridge in col.12, lines 11-13, col.13, lines 26-43) from south bridge.

6. As to claim 3, Wandler□s north bridge [50], CPU and the memory were also integrated on a substrate (e.g. see the integrated feature of the north bridge 50 to memory and CPU in col. 6, lines 1-27).

7. As to claim 4, Wandler also included graphic controller [60] for requesting data to the north bridge at graphic controller's rate (e.g. see the rapid retrieval of he data in col.6, lines 28-52).

8. As to claim 14, Wandler also included at least :

a) memory that is contained in substrate [10] (see fig.2);

b)north bridge [50] operable coupled to interface with memory [75] , wherein the north bridge included a memory access request buffer(see fig.4) interoperable coupled with a memory controller [504] (fig.4), wherein the memory access request buffer received memory access request (e.g. see the read/write queues 508 510 in col.11, lines 60-67, col.12, lines 1-10), wherein the memory controller retrieve the request from the buffer (e.g. see the read/write queues 508, 510,512,514 in col.11, lines 60-67, col.12, lines 1-10) and processed the request;

c)memory bus [27] coupled to the north bridge [50] (e.g. see fig.4).

9. Wandler did not specifically show retrieving the request at the memory rate as claimed. However, Sakugawa disclosed a system for processing requests where a memory controller 2 is shifted to the waiting state in response to the memory access

request from a cpu [CPU] which was allowed to be operated at a low speed, the external device 32 which is to be operated at a high speed must wait for a period equivalent to the waiting time of the memory controller 2 (see the waiting period of the memory controller in col. 3, lines 1-14, col.5 lines 5-46, see also col.7, lines 5-25). The reasons of obviousness which are applicable to both claims 1 and 14 have been given in paragraph # 4 above, therefore, it will not be repeated herein.

10. As to claim 18, Wandler also included PCI bus (e.g. see fig.2 PCI).

11. As to claim 19, Wandler also included a device bus (e.g. see fig.2 connection to peripheral device).

12. As to claim 29, Wandler also buffering the request by the north bridge 50 from south bridge (see fig.4).

13. As to claim 30, Wandler also integrating the CPU , north bridge and south bridge (see PCI bus in fig.2, see also col.6, lines 5-7 for integrating the north bridge into CPU).

14. As to claim 31, Wandler also included graphic controller [60] for requesting data to the north bridge at graphic controller's rate (e.g. see the rapid retrieval of he data in col.6, lines 28-52).

15. Claims 5,6, 32,33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wandler et al. (5,991,833) in view of Sakugawa et al. (6,684,278) as applied to claim 1 and clam 28 above, and further in view of Onishi et al. (5,845,329).

16. As to claims, 5,6, 32,33, neither Wandler nor Sakugawa specifically show the translation of the virtual to physical address of the request as claimed. However, Onishi

disclosed a system translating a virtual address into physical address of a memory request (e.g. see col.10, lines 4-13). It would have been obvious to one of ordinary skill in the art o use Onishi in Wandler for translating the virtual and physical address as claimed because the use of Onishi could enhance the processing capability of Wandler to adjust to particular requirements of the memory access at a predetermined format, such as virtual and physical addresses, and it could be readily done by predefining the translation variables, such as address range of the read/write operation, of Onishi into Wandler□s configuration file such that the mapping of the virtual and physical addresses could be recognized by Wandler, and because one of ordinary skill in the art should be able to recognize the need for converting the virtual and physical addresses as Wandler also taught that his memory was a DRAM type memory (col.6, lines 21-27), which was a storage of a physical address array, and in doing so , provided a motivation.

17. Wandler et al. (5,991,833) and Onishi et al. (5,845,329) were cited to applicant in a previous office action, therefore, copies of these patent are not provided herein.

18. claims 7-13, 20-27 would be allowable over the art of record for specifically showing the combined features of the functional elements of the instruction module, cache modules , decoder and phase locked loop and the memory access request received from the central processing unit at operational rate of the central processing unit and the memory access request received from the request buffer at the memory rate, the memory access request when information relating to executing one of the

operational instructions was not stored in the data module or the instruction module and the north bridge for the operating rate of the central processing unit and for the operating rate of the memory.

19. Claims 15-17 are objected for being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined elements of the data module, instruction module, phase locked loop, the request issued at the operating rate of the CPU, the memory access request when information relating to executing one of the operational instructions was not stored in the data module or the instruction module and the north bridge at the operating rate of central processing unit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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